Amendments to the Specification

Please replace the paragraph on page 6, lines 10-17 with the following amended paragraph:

The disclosed control register **102** provides an offset value and a bit that controls whether the offset value is added to or subtracted from the delay value **106** determined by the DLL **100**. With these modifications, an additional controller (hardware or software, not shown) may be added to run a memory test while adding and subtracting various offsets ~~110~~ **11** to determine the limits of failure free operation. The final offset ~~110~~ **11** to be used in normal operation is preferably the one in the middle of the limits in which the memory test passes.

Please replace the paragraph on page 6, lines 23-28 with the following amended paragraph:

One important advantage provided by this embodiment of the present invention is that the data strobe (DQS) delay can be tweaked by the addition or subtraction of a fine adjustment offset ~~110~~ **11**, to allow it to be positioned closer to the actual, optimal center of the data eye. This results in more reliable memory operations, as well as a higher frequency of operation.

Please replace the paragraph on page 7, lines 4-19 with the following amended paragraph:

In particular, Fig. 2 shows a modification to the circuit shown in Fig. 1 wherein a PVT circuit **200** is added to compensate for changes in the tweaked delay value providing offset ~~110~~ **11** due to fluctuations in voltage and temperature. PVT circuits are known, and provide information about the operating conditions (process, voltage, and temperature) of a device in a system. The PVT circuit **200** outputs another fine adjustment offset output value **211** that indicates the current operating conditions of the device. The PVT fine adjustment offset output value **211** will vary as the actual voltage and/or temperature changes. The PVT fine adjustment offset output value **211** is also affected by actual variations in the device process manufacturing, which can be considered a constant for any given instance of a device. As applied to the present invention, the PVT circuit **200** corrects the offset delay ~~110~~ **11** provided by the DLL **100a**, and the offset ~~110~~ **11** provided by the control register **102**, keeping the overall actual delay offset relatively constant as the voltage and/or temperature of the DDR read data capture circuit actually varies over time.